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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,095	12/29/2000	Stephan J. Jourdan	2207/7083	6387

25693 7590 05/05/2006

KENYON & KENYON LLP
RIVERPARK TOWERS, SUITE 600
333 W. SAN CARLOS ST.
SAN JOSE, CA 95110

EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/05/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/750,095
Filing Date: December 29, 2000
Appellant(s): Stephan J. Jourdan et al.

Sumit Bhattacharya
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 21, 2006 appealing from the Office action mailed July 18, 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect. While it is correct that the included appendix reflects the present status of the claims, 37 CFR § 41.37 requires that this be the case in regards to the appendix.

The correct statement that appellant should have made in this section is: No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is substantially correct. It should be noted that while the summary of claimed subject matter appears to comply with the letter of 37 CFR § 41.37(c)(1)(v) in that it lists the claimed material and refers to the specification by page and line numbers and to the drawings by reference character, it fails to comply with the spirit of the rule. The existing summary amounts to nothing more than a verbatim copy of the claim with inserted parenthetical expressions referencing the specification and drawing. No "explanation" of the claimed material is provided.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct. It is noted that appellant has provided a complete copy of the claims listing while appeal is sought only for claims 13-14 and 16-18.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

US 5,758,112 Yeager et al. 05-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 13-14 and 16-18 are rejected under 35 U.S.C. § 102(b) as being clearly anticipated by Yeager et al., U.S. Patent 5,758,112.

Yeager et al. taught (e.g. see figs. 1-9b) the invention as claimed (as per claim 13), including a data processing ("DP") system comprising:

13. A method for recovering registers in a processor, comprising:	col. 2 lines 40-42 - This section of Yeager et al. describes "saving and restoring register-renaming information", the "restoring register-renaming information" being that which is equivalent to the claimed "recovering registers" because when register-renaming information is "restored" a previous mapping of operands to registers is "recovered" in the processor.

reading a bit in an active list;	col. 15 line 61 to col. 16 line 14 - This section of Yeager et al. describe "done bit 286" and "exception bit 288", which are shown on fig. 2 as being present in "active list" 212. Col. 15 lines 64-65 state that: "The 'done' and 'exception' bits control when instructions graduate." Col. 15 lines 63-64 state that: "These bits [referring to the done and exceptions bits] are set when an instruction completes execution." Col. 16 lines 1-3 state that: "Instructions graduate in original program order from active list 212, after they have been completed by a functional unit. Because execution and completion can occur out of order, each completion is recorded by setting done bit 286 for that instruction." Col. 16 lines 9-12 state that: "As instructions graduate, a 'graduation unit' (not shown) removes instructions from active list 212 and appends their old destination registers to free lists 208 or 210 for re-use." As seen above, in order for the system to graduate instructions after those instructions have completed, and in order for this completion to occur "out of order" while graduation occurs "in original program order", the "graduation unit" which was not shown by Yeager et al. must inherently **read** the done bit in order to determine if a next instruction in "original program order" is eligible to graduate. This inherent reading of the done bit anticipates claim 13's language of simply reading "a" bit in "an active list" because the done bit is "a" bit, and it it in an "active list" (fig. 2, 212, 276).

reclaiming a physical register from a new field of said active list to a free list according to said bit; and	col. 16 lines 1-14 - This section of Yeager et al. describes the graduation process of Yeager et al.'s system. Specifically, lines 9-14 detail that a "graduation unit" (which was not shown by Yeager et al.) has the function of "remov[ing] instructions from active list 212 and append[ing] their old destination registers to free lists 208 or 210 for re-use. From appellant's specification, at pg. 7 line 24, is found appellant's description of what is meant by the claimed "new field": "New field 310 may contain the newly mapped physical register by the RAT 302 for each renamed instruction. For example, instruction 1 specifies logical register EAX as its destination physical register. RAT 302 evicts physical register R1 to old field 308 and maps logical register EAX for instruction 1 to physical register R2. This mapping is recorded in new field 310." As seen from the above quote, the intended meaning of "new field" is a current destination register mapping while the instruction is active. In Yeager et al., because his description of the graduation process is after the instruction has completed, he refers to what was that instructions "current destination register mapping" as "old destination registers". However, because these "old destination registers" were the current mappings for the instruction when it was executing (col. 7 line 64 to col. 8 line 18), they have the exact same meaning as the meaning for the claim term "new field" based upon appellant's specification. Accordingly, appellant's claim term "new field" is equivalent to Yeager et al.'s "old destination registers" term because the underlying meanings are the same.

setting said bit during a misprediction condition.	col. 17 lines 20-50 - This section of Yeager et al. describes how when a "branch is reversed", the "active list" "must be restored to the point at which the execution paths diverged". Yeager et al.'s meaning of "branch is reversed" is found at col. 4 lines 15-27, specifically lines 19-27 which state: "As discussed below, processor 100 can execute a conditional branch speculatively by predicting the most likely path and decoding instructions along that path. The prediction is verified when the condition becomes known. If the correct path was taken, processing continues along that path. **Otherwise, the decision must be reversed**, all speculatively decoded instructions must be aborted, and the program counter and mapping hardware must be restored." As seen from the above section of Yeager et al., the meaning of "branch is reversed" is when the system has performed an incorrect prediction of a branch. Appellant's intended meaning of "misprediction" can be found from pg. 7 line 30 to pg. 8 line 2 of the specification, where it states: "A misprediction condition may occur that impacts register renaming structure 300. For example, instruction 3 may be a branch instruction having a predicted result. If the prediction is in error, then the branch is "mispredicted" and a misprediction condition occurs. Instructions executed after the misprediction are flushed because they are incorrect." As seen from the quote above, appellants intended meaning for "misprediction condition" is a branch which is incorrectly predicted. This is exactly the same meaning as Yeager et al.'s "branch reversal" above. Therefore, Yeager et al.'s term "branch is reversed" is a "misprediction condition" as claimed because the underlying meanings for the terms are identical. Accordingly, when Yeager et al. restores the active list as a result of a misprediction (branch reversal in Yeager et al.), this restoration of the active list to a previous state will set all bits of the active list, including the done bit and exception bit, to the state that the bits existed in at the time the branch was mispredicted. This is a "set[ting]" of the bit during a misprediction condition as claimed.

As to claim 14, Yeager et al. taught overwriting an entry in said active list (col. 16 lines 30-50).

As to claim 16, Yeager et al. taught that said reclaiming included reading said physical register from an old field in said active list (col. 16 lines 37-50).

As to claim 17, Yeager et al. taught that said reclaiming included reading said physical register from a new field in said active list (col. 16 lines 37-50).

As to claim 18, Yeager et al. taught that the reading included reading a bit in a bit field within said

active list (col. 16 lines 1-14).

(10) Response to Argument

At pg. 7 of the brief, appellant argues:

> "In the original rejection of independent claim 13, the Examiner asserted that Yeager teaches a method for recovering registers in a processor (col. 2, lines 40-42); reading a bit in an active list (col. 15, line 61 to col. 16 line 14); reclaiming a physical register from said active list to a free list according to said bit (col. 16, lines 1-14). *See* page 3, Office Action dated 12/9/2003. Applicants disagree. Column 2, lines 40-42 state:
>
> "The present invention offers a highly efficient mechanism for saving and restoring register-renaming information to facilitate branch prediction and speculative execution."
>
> The cited section of Yeager does not disclose at least a reclaiming a physical register from a new field of said active list to a free list according to said bit; and setting said bit during a misprediction condition as specifically described in the embodiment of claim 1. [sic, presumably appellant meant claim 13 here]."

This argument is not persuasive because as is clearly seen from the rejection above, col. 2 lines 40-42 were recited to show that Yeager et al. taught the claim text of "A method for recovering registers in a processor". Appellant's arguments are that the cited section does not also read upon the remainder of the claim. That argument is incorrect because other sections of Yeager et al. were cited to read upon the other claim elements recited as detailed in the rejection above. The detailed explanation provided in the rejection of claim 13 above explaining how Yeager et al. taught recovering registers in a processor is herein incorporated by reference.

At pg. 7 of the brief, appellant argues:

> "Column 15, lines 61-67 state:
>
> [lengthy repetitive quote of col. 15 lines 61-67 of Yeager et al. omitted]
>
> The cited section discloses the "done" and "exception" bits of Yeager, but again does not disclose at least reclaiming a physical register from a new field of said active list to a free list according to said bit; and setting said bit during a misprediction condition, or any equivalent thereof, as specifically described in the embodiment of claim 13.

Appellant again repeats the same error committed in the previous argument in that appellant argues that col. 15 lines 61-67 of Yeager et al. do not teach the "reclaiming" and "setting" steps of claim 13. However, Yeager et al. col. 15 lines 61-67 were cited to show that Yeager et al. taught the "reading a bit in

an active list" claim limitation as detailed in the rejection above. Other sections of Yeager et al., as detailed in the rejection above, were cited to show that Yeager et al. taught the "reclaiming" and "setting" steps of claim 13. The detailed analysis of how Yeager et al. anticipates the "reading a bit in an active list" limitation of claim 13 is herein incorporated by reference.

At pg. 7 of the brief, appellant argues:

"Finally, Column 16 lines 1-14 state:

[lengthy repetitive quote of Yeager et al. col. 16 lines 1-14 omitted]

The cited section discloses the utility and operation of the "done bit" and a "graduation unit" of Yeager in the completion of instructions, but fails to disclose at least reclaiming a physical register from a new field of said active list to a free list according to said bit; and setting said bit during a misprediction condition or any equivalent thereof."

In this argument, appellant again makes the same error as the previous two arguments, in that appellant relates the cited section of Yeager et al. to the "setting" step of the claim language when the cited section was cited to show that Yeager et al. taught the reclaiming step of the claim. Furthermore, the rejection above clearly details exactly how Yeager et al. taught the claimed feature of "reclaiming" and the discussion provided therein is incorporated herein by reference.

At pg. 8-9 of the brief, appellant argues that claim 13 contains similar limitations to allowed claim 1 and therefore should also be allowable. However, appellant is failing to recognize that claim 13 is significantly broader in scope than claim 1 and is therefore anticipated by Yeager et al. while claim 1 contains other limitations not present in claim 13 that make it (claim 1) allowable over Yeager et al.

At pg. 9 of the brief, appellant argues:

"In particular, Applicants submit that the cited sections do not teach *reclaiming a physical register from a new field of said active list to a free list* according to said bit; and setting said bit *during a misprediction condition.*"

This argument is not persuasive because as has been clearly detailed in the rejection above, Yeager

et al. did in fact teach these very steps. The detailed explanation provided in the rejection above for the "reclaiming" and "setting" steps of claim 13 are incorporated herein by reference.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Richard Ellis

RICHARD L. ELLIS
PRIMARY EXAMINER

Conferees:

Eddie Chan, SPE

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Donald Sparks, SPE

DONALD SPARKS
SUPERVISORY PATENT EXAMINER